Design and Comparison of Two High Power-Supply Rejection Capacitor-less Low-Dropout Regulators Using a Voltage Subtractor Stage

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***Abstract*—Two high power-supply rejection capacitor-less low-dropout (LDO) regulators are proposed, simulation were performed in order to characterize the circuit. The main difference between both regulators is the error amplifier, one have PMOS transistors as the differential pair, while the other have NMOS transistors. Both LDO regulators have a voltage subtractor stage to achieve high power-supply rejection (PSR). Also, they use on-chip capacitors, allowing full integration. The regulators were designed in a CMOS 0.18-um process from TSMC. The system has an output voltage of 1 V, dropout voltage of 0.2 V and maximum load current of 100 mA. The first LDO has PSR of -28 dB at 100 kHz with the compensation capacitor of 9 pF. The second LDO have PSR of -53 dB at 100 kHz with a 17.4 pF compensation capacitor.**

***Index Terms*—low dropout regulator, power-supply rejection, capacitor-less, power management, voltage subtractor stage.**

I. Introduction

In the last decades the use of portable electronic devices has grown, and with the portability nature of such devices many interest on efficient power management has emerged. One common solution for a efficient power management system is to integrate all necessary components into a system-on-chip (SoC) solution, achieving high efficiency [1].

Typically, a power management system comprises a DC-DC switched converter followed by a low-dropout voltage regulator, as shown in Fig. 1. Due to its switching nature, the DC-DC converter have high output ripple. In order to reduce the ripple an LDO regulator is inserted in the system, what provides stable voltage to Digital/RF/Analog blocks to operate properly. The metric that defines the ability of a LDO regulator to reject ripple from its supply is called Power-Supply Rejection (PSR) [2].

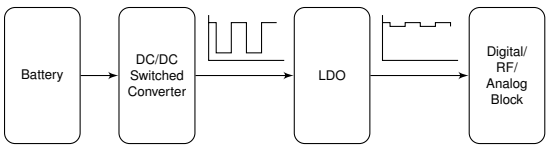

Fig. 1. Block diagram of a typical power management system used in SoCs.

In this paper the topology of two LDO regulators with high PSR for SoC application are proposed. In section II the basic LDO regulator operation is presented. Section III features current techniques to improve PSR highlighting the one applied in this paper. Section IV present the two proposed architecture and details its design. The comparison of the simulation results are discussed in Section V and conclusions are draw in Section VI.

II. Typical LDO Regulator

A circuit diagram of a typical LDO regulator is illustrated in Fig. 2. The three main blocks are: (1) a PMOS transistor M_P known as the pass transistor, (2) an operational amplifier known as error amplifier (EA) and (3) a feedback network [1], represented by the resistors R_{F1} and R_{F2}.

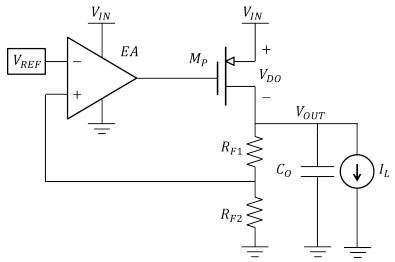

Fig. 2. Circuit diagram of typical LDO regulator.

In the same figure, V_{REF} is a reference voltage, V_{DO} is the dropout voltage, C_O an output capacitance and the load is modeled by the current source I_L. The output voltage is given by:

$$V_{OUT} = \left(\frac{R_{F1} + R_{F2}}{R_{F2}}\right) V_{REF}. \quad (1)$$

The feedback network sends to the error amplifier a sample of V_{OUT}, if this sample differs from V_{REF} the EA modulates the conductivity of the pass transistor, therefore regulating the output voltage.

The LDO regulator has multiple poles and hence it have to be compensated. Generally, the output capacitance C_O is

used to balance the regulator. The problem with this approach is that the order of such capacitor is of several micro-farads, what is not suitable for SoC application. Therefore a different compensation technique must be used [3]. This type of LDO regulators are known as capacitor-less LDOs and C_O models an output parasitic capacitance.

III. Power-Supply Rejection

The PSR is function of frequency and represents the small signal gain from V_{IN} to V_{OUT}. Letting v_{out} and v_{in} be the small signal voltages at the output and input, respectively, the PSR is:

$$PSR(f) = \frac{v_{out}}{v_{in}}. \tag{2}$$

To improve the PSR of LDO regulators many techniques can be found in literature, for example in [4] and [5], however some of these methods can increase the area and the drop-out voltage (V_{DO}), other techniques that uses feed-forward ripple cancellation can overcome these disadvantages and will be discussed later [6].

Fig. 3 can be used to find the LDO regulator PSR, where A_{EA} represents the gain of EA, A_P represents the gate to drain gain of M_P, A_{Pdd} is the source to drain gain of M_P, A_{EAdd} represents the PSR of EA and β is the feedback factor. The reference voltage V_{REF} is provided by a band-gap reference, the influence of this circuit in the LDO PSR can be eliminated by designing a band-gap reference with high PSR or using a filter. Considering an ideal reference voltage the PSR of a LDO regulator can be described as:

$$PSR = \frac{A_{Pdd}(s) + A_P(s)A_{EAdd}(s)}{1 + \beta A_P(s)A_{EA}(s)}. \tag{3}$$

Let gm_P and r_{0P} represent the PMOS transistor (M_P) small signal transconductance and output resistance, respectively, and let R_{OUT} be the parallel resistance of the load resistance, the sum of the feedback resistors R_{F1} and R_{F2} and r_{0P}. The PMOS DC source to drain gain and DC gate to drain gain are given by:

$$A_{Pdd}(0) = \left(gm_P + \frac{1}{r_{0P}}\right) R_{OUT} \tag{4}$$

and

$$A_P(0) = -gm_P R_{OUT}. \tag{5}$$

If we replace both equations (4) and (5) into (3), then the LDO DC PSR can be calculated by:

$$PSR = \frac{R_{OUT}[1/ro_P + gm_P(1 - A_{EAdd})]}{1 - \beta gm_P R_{OUT} A_{EAE}}. \tag{6}$$

According to equation (6) the design of the EA with $A_{EAdd} = 1 + (gm_P r_{0P})^{-1}$ leads to $PSR = 0$ and the LDO DC PSR would get a great improvement, however $gm_P r_{0P}$ is the PMOS intrinsic gain, which is function of $\sqrt{I_{LOAD}}$. Therefore, A_{EAdd} must change with I_{LOAD} what is difficult to achieve with common EA topology [7].

Designing an EA with $A_{EAdd} \approx 1$ is possible and also increases the PSR, this can be done using a voltage subtractor stage [8]. It is intuitive to visualize this technique because it consists of reproducing the ripple in the PMOS transistor gate making the source-gate voltage constant. Also, this can be done in a wide frequency range by using a filter that copy the ripple in the gate terminal of the pass transistor. This technique is known as *feed-forward ripple cancellation* [6].

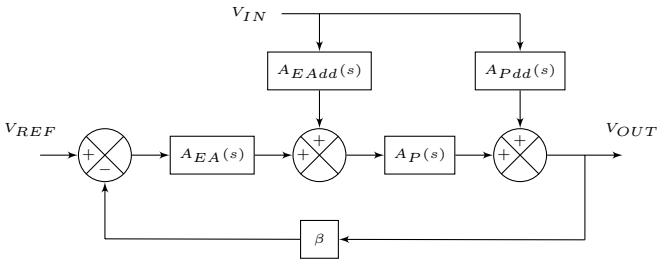

Fig. 3. LDO regulator block diagram for PSR analysis.

IV. High PSR LDO Regulators Design

A. Topologies Description

The two proposed high PSR LDO regulator topologies that uses a voltage subtractor stage are illustrated in Fig. 4 and Fig. 5, they will be called LDO_1 and LDO_2, respectively. In both topologies, transistor M_1 to M_{14} forms the error amplifier, M_P is the pass transistor and for LDO_1, transistors M_{15} and M_{16} forms the feedback network, LDO_2 applies unit feedback, $\beta = 1$. Capacitor C_C is used to achieve stability by applying the Miller compensation technique [9].

Both LDO regulators have a three stage error amplifier. The first stage comprises current source I_{B1} and transistors M_1 to M_{10}, which forms a folded-cascode stage, responsible for provide high gain and its high output impedance is used to compensate the circuit, voltages V_{B1}, V_{B2} and V_{B3} are provided by a bias circuit. The second stage comprises current source I_{B2} and transistors M_{11} and M_{12}, those components forms a wideband amplifier, used to provide gain to minimize the compensation capacitor C_C, it need to be a wideband amplifier to push its output pole to high frequencies, not compromising stability [4], therefore M_{12} is required to decrease the output resistance, increasing its output pole. The first and second stage, on each LDO regulator, were chosen in a way that approximately no ripple appears in V_{OUT2}.

The third stage is formed by transistors M_{13} and M_{14}, it's the voltage subtractor stage responsible for provide $A_{EAdd} \approx 1$. The diode-connected transistor M_{14} has small output resistance, equals to the inverse of its transconductance, $1/gm_{14}$. Letting v_{out3} be the small signal voltage in V_{OUT3}, we can find gain v_{in}/v_{out3} using a voltage divider,

$$\frac{v_{IN}}{v_{OUT3}} = \frac{r_{013}}{r_{013} + 1/gm_{14}} \tag{7}$$

where r_{013} is M_{13} small signal output resistance, since r_{013} is much greater than $1/gm_{14}$ and knowing that approximately no ripple appears in V_{OUT2}, we have $A_{EAdd} \approx 1$.

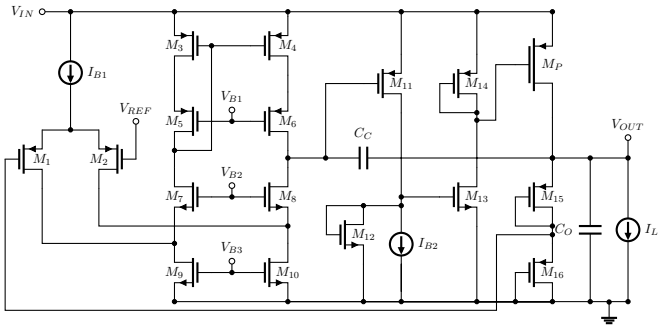

Fig. 4. High PSR LDO regulator using PMOS transistors in the EA differential pair.

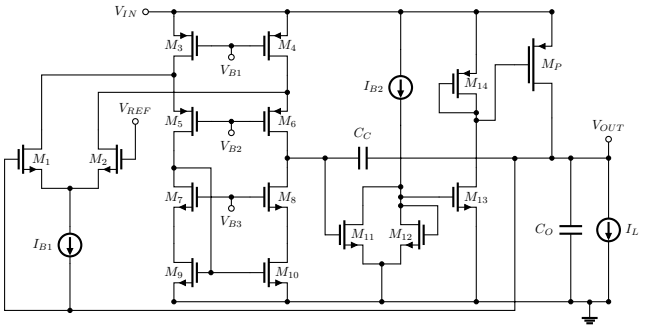

Fig. 5. High PSR LDO regulator using NMOS transistors in the EA differential pair.

B. Transistor-level Design

The topologies from Fig. 4 and Fig. 5 were designed using the CMOS $0.18\,\mu m$ technology from TSMC on Cadence® Virtuoso® software. Both LDO regulators were design to provide $V_{OUT} = 1\,V$ and a maximum load current of $100\,mA@$ $V_{DO} = 200\,mV$. If not emphasized, all the steps were taken for both regulators.

All MOSFETs used in the design were the standard $1.8\,V$ nominal V_T transistors. The NMOS transistors bulks were connected to groud, as it should, but in the PMOS transistors, each bulk was connected to source to avoid body effect. To eliminate inaccuracies due to second-order effects caused by transistors having non-equal widths, all EA transistors are parallel combinations of a unit-size transistor. M_1 and M_2 were biased in moderate inversion while all the others EA transistors were biased in strong inversion. The width and length of this unit-size transistor were chosen based on its intrinsic gain, the EA first stage gain equation, which is the one for a folded-cascode op amp and its current consumption. The quadratic equation for a MOSFET operating in saturation region was used to model the unit-size transistor behavior, the parameters were extracted to realize analytical hand calculations and find the width of each transistor, when needed the width was adjusted by simulation to reach the specifications.

The PMOS transistor M_P was designed to operate in strong inversion on the boundary of the saturation region when it supplies maximum load current with minimum length. The feedback network transistors M_{15} and M_{16} were chosen as PMOS transistors to avoid body effect and they were designed to consume $10\,\mu A$ in strong inversion while operating in saturation region.

The compensation technique used on the regulators presents a problem known as high Q problem which limits the minimum load current that allows stability [10]. Therefore, with $1\,mA$ as minimum load current, searching for $45°$ phase margin, capacitor C_C value was found by parametric simulation. This value was found assuming a worst case scenario for the parasitic output capacitance $C_O = 100\,pF$.

Using all previous considerations, the EA unit-size transistor length and width are $1.5\,\mu m$ and $1\,\mu m$, respectively, the pass transistor width is $5.2\,mm$. For LDO_1 the compensation capacitor value is $9\,pF$ and for LDO_2, the value is $17.4\,pF$. Both bias currents I_{B1} and I_{B2} are $40\,\mu A$, the third stage was biased at first as $5\,\mu A$, it should be noted that this current varies with load current. All the EA transistors widths are shown in Table I. The EA gain frequency response can be observed in Fig. 6, note that the first pole appears in a higher frequency on the LDO_2.

TABLE I
ERROR AMPLIFIER TRANSISTORS WIDTHS.

Transistor	***Width* (µm)** LDO_1-LDO_2	***Transistor***	***Width* (µm)** LDO_1-LDO_2
M_1	190-100	M_5	49-21
M_2	190-100	M_6	49-21
M_3	22-30	M_7	5-5
M_4	22-30	M_8	5-5
M_9	10-1	M_{13}	1-1
M_{10}	10-1	M_{14}	5-3
M_{11}	178-10	M_{15}	25
M_{12}	2-1	M_{16}	25

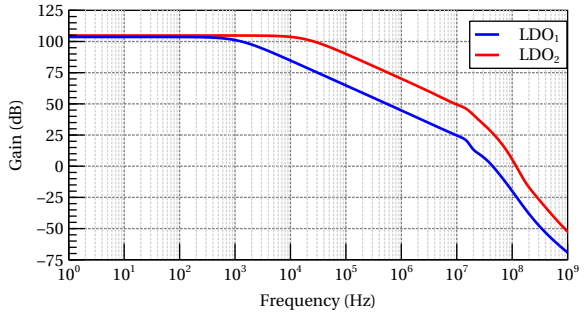

Fig. 6. Error Amplifier frequency response for both LDO regulators.

V. Simulation Results

All results were obtained via simulation and performed with Cadence® Spectre® software. With the parameters found in Section IV, the LDO regulators were able to provide $V_{OUT} = 1\,V$ with $100\,mA@V_{DO} = 200\,mV$ and presented approximately a phase margin of $50°$ when supplying minimum load current with a $100\,pF$ output parasitic capacitance.

TABLE II
KEY PERFORMANCE PARAMETERS COMPARISON.

Parameter	LDO_1	LDO_2	**[3]**	**[11]**	**[6]**
CMOS Technology	0.18 µm	0.18 µm	0.6 µm	0.18 µm	0.13 µm
V_{OUT} (V)	1	1	2.8	1.8	1
V_{DO} (mV)	200	200	300	200	150
I_Q (µA)	< 100	< 100	< 100	< 193	< 50
$I_{L,min} - I_{L,max}$ (mA)	$1 - 100$	$1 - 100$	$0.1 - 50$	$0.05 - 50$	$X - 25$
R_C (µV/mA)	5.2	18.16	842	30.6	48
R_L (µV/V)	1	2.2	2000	1.66	X
PSR (dB) @100 kHz	-28	-53	-26	-52	-60
C_C (pF)	9	17.4	2.8	5.7	5
$Noise$ (μV_{RMS}) (from 100 Hz to 100 kHz)	23.36	7.66	106	X	X

The LDO regulators PSR were simulated for maximum and minimum load current, ideal resistors were used as load instead of current source I_L. The results are illustrated in Fig. 7, observe that the results of LDO_2 are superior most because its PSR starts to decrease in a greater frequency than LDO_1.

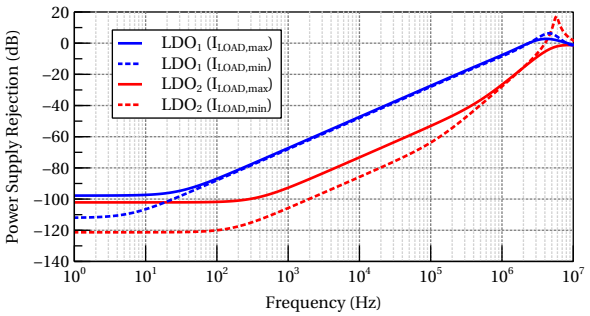

Fig. 7. PSR performance for both LDO regulators.

Three factors contributes to this difference, the EA frequency response, the feedback network and the fact that the first stage output of LDO_1 replicates the ripple presented in V_{IN} while in the LDO_2 it is approximately zero. When the impedance of capacitor C_C start to decrease due to an increase in the ripple frequency, the ripple presented on the first stage output flows to the LDO_2 output, what does not happen on the LDO_1.

A comparison summary is presented in Table II for the designed regulators and other LDOs with PSR enhancement. In this table I_Q is the quiescent current, R_C the load regulation and R_L the line regulation. It is important to point out that the results of [3] and [6] are measures, while the other are simulations.

Although the LDO_2 performs better than LDO_1, the fact that it needs a compensation capacitor with an area twice bigger than the one needed for the LDO_1 is an important drawback and need to be referenced as a design constraint.

VI. CONCLUSION

From Table II it can be seen that the LDO regulators designed in this work achieve good PSR performance at low frequencies due to the EA frequency response. If area is not a design constraint, the topology of choice should be LDO_2 due to its higher PSR. Also, the use of the voltage subtractor stage is simple and enhances the design since it ameliorate the DC PSR without the necessity of significant increases in area nor V_{DO}.

REFERENCES

[1] M. Gupta and R. K. Sharma, "Design of Output Capacitorless Low Dropout Regulator with Fast Transition Response," 2018 Second International Conference on Intelligent Computing and Control Systems (ICICCS), Madurai, India, 2018, pp. 995-998, doi: 10.1109/ICCONS.2018.8662995.

[2] A. P. Patel and G. A. Rincón-Mora, "High Power-Supply-Rejection (PSR) Current-Mode Low-Dropout (LDO) Regulator," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 57, no. 11, pp. 868-873, Nov. 2010, doi: 10.1109/TCSII.2010.2068110.

[3] J. Torres et al., "Low Drop-Out Voltage Regulators: Capacitorless Architecture Comparison," in IEEE Circuits and Systems Magazine, vol. 14, no. 2, pp. 6-26, Second quarter 2014, doi: 10.1109/MCAS.2014.2314263.

[4] K. Wong and D. Evans, "A 150mA Low Noise, High PSRR Low-Dropout Linear Regulator in 0.13um Technology for RF SoC Applications," 2006 Proceedings of the 32nd European Solid-State Circuits Conference, Montreux, 2006, pp. 532-535, doi: 10.1109/ESSCIR.2006.307507.

[5] V. Gupta and G. A. Rincon-Mora, "A low dropout, CMOS regulator with high PSR over wideband frequencies," 2005 IEEE International Symposium on Circuits and Systems, Kobe, 2005, pp. 4245-4248 Vol. 5, doi: 10.1109/ISCAS.2005.1465568.

[6] M. El-Nozahi, A. Amer, J. Torres, K. Entesari and E. Sanchez-Sinencio, "High PSR Low Drop-Out Regulator With Feed-Forward Ripple Cancellation Technique," in IEEE Journal of Solid-State Circuits, vol. 45, no. 3, pp. 565-577, March 2010, doi: 10.1109/JSSC.2009.2039685.

[7] Yali Shao, Yi Wang, Zhihua Ning and Lenian He, "Analysis and design of high power supply rejection LDO," 2009 IEEE 8th International Conference on ASIC, Changsha, Hunan, 2009, pp. 324-327, doi: 10.1109/ASICON.2009.5351438.

[8] S. K. Hoon, S. Chen, F. Maloberti, J. Chen and B. Aravind, "A low noise, high power supply rejection low dropout regulator for wireless system-on-chip applications," Proceedings of the IEEE 2005 Custom Integrated Circuits Conference, 2005., San Jose, CA, 2005, pp. 759-762, doi: 10.1109/CICC.2005.1568779.

[9] Ka Nang Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," in IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 48, no. 9, pp. 1041-1056, Sept. 2001, doi: 10.1109/81.948432.

[10] S. K. Lau, P. K. T. Mok and K. N. Leung, "A Low-Dropout Regulator for SoC With Q-Reduction," in IEEE Journal of Solid-State Circuits, vol. 42, no. 3, pp. 658-664, March 2007, doi: 10.1109/JSSC.2006.891496.

[11] W. Xu, G. Wang, J. Jiang, X. Qi, and F. Zhang, "A high-PSR transient-enhanced output-capacitor less CMOS low-dropout regulator for SoC applications," Int. J. Electron., vol. 98, no. 10, pp. 1319–1332, Oct. 2011.